UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,148	07/25/2001	Michael R. Buckmaster	120073.415D1	1898

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EXAMINER
GUILL, RUSSELL L

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<table>
<tr>
<td rowspan="2">Office Action Summary</td>
<td>Application No.
09/916,148</td>
<td>Applicant(s)
BUCKMASTER ET AL.</td>
</tr>
<tr>
<td>Examiner
Russell L. Guill</td>
<td>Art Unit
2123</td>
<td></td>
</tr>
</table>

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 July 2001</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>22 -28</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>25 July 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____ | page

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 22 – 28 have been examined. Claims 22 – 28 have been rejected.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure:

2.1.   The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

2.2.   The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it is more than 150

words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and
> distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 22 - 28 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the

subject matter which applicant regards as the invention. Regarding claim

22, the preamble of claim 22 recites, "the target processor being coupled to

the target hardware that may be partially physical and partially simulated".

However, the claim limitations appear to be directed at target hardware that

is partially physical and partially simulated. The claims are indefinite

because it is unclear what is intended by the phrase "may be" in the

preamble. For the purpose of claim interpretation, the phrase "may be" is

interpreted as "is".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102

that form the basis for the rejections under this section made in this Office

action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen (U.S. Patent 5,790,881).

7.1.   Nguyen reads directly on the claim 22 *(Title, and figure 1, and column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract)*. Nguyen describes a coprocessor that simulates a memory interface to a master device, in addition to physical memory.

7.1.1. Regarding *(Title, and figure 1, and column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract)*; it is inherent that an address decode is performed to select either physical memory or the simulated memory. This decode process monitors signals from the target processor, and determines when the target processor is attempting to access the simulated memory. Further, the wait condition suspends execution of the target processor (and program).

8. Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen

(U.S. Patent 5,790,881).

8.1. Claim 23 is a dependent claim of claim 22, and thereby inherits all of

the rejected limitations of claim 22.

8.2. Nguyen reads directly on the claim 23 ***(Title, and figure 1, and***

column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract).

Nguyen describes a coprocessor that simulates a memory interface to a

master device, in addition to physical memory.

8.2.1. Regarding ***(Title, and figure 1, and column 1, lines 65 – 67,***

and column 2, lines 1 – 21, and Abstract); it is inherent that an

address decode is performed to select either physical memory or the

simulated memory. This decode process monitors signals from the

target processor, and determines when the target processor is

attempting to access the physical memory, and allows the access.

9. Claim 24 is rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen

(U.S. Patent 5,790,881).

9.1. Claim 24 is a dependent claim of claim 22, and thereby inherits all of

the rejected limitations of claim 22.

9.2. Nguyen reads directly on the claim 24 *(Title, and figure 1, and column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract).* Nguyen describes a coprocessor that simulates a memory interface to a master device, in addition to physical memory.

9.2.1. Regarding *(Title, and figure 1, and column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract)*; it is inherent that input data in the coprocessor is converted to input signals.

10. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen (U.S. Patent 5,790,881).

10.1. Claim 25 is a dependent claim of claim 22, and thereby inherits all of the rejected limitations of claim 22.

10.2. Nguyen reads directly on the claim 25 *(Title, and figure 1, and column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract).* Nguyen describes a coprocessor that simulates a memory interface to a master device, in addition to physical memory.

10.2.1. Regarding *(Title, and figure 1, and column 1, lines 65 – 67, and column 2, lines 1 – 21, and Abstract)*; it is inherent that an address decode is performed to select either physical memory or the simulated memory. The address decode compares an address on the address bus against the address range of the coprocessor. In

order to build the address decoder, it is inherent that the addresses

of the coprocessor were recorded in the structure of the address

decoder.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or
> described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made to a
> person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Nguyen (U.S. Patent 5,790,881) in view of Mano (Mano, M. Morris;

"Computer System Architecture", 1982, Prentice-Hall).

12.1. Claim 26 is a dependent claim of claim 22, and thereby inherits all of

the rejected limitations of claim 22.

12.2. The art of Nguyen is directed toward a computer system including

coprocessor devices simulating memory interfaces *(Title)*.

12.3. The art of Mano is directed to computer system architecture *(Title)*.

12.4. Nguyen does not specifically teach monitoring a terminal on the target processor that is adapted to receive a control signal from the physical hardware by the target processor.

12.5. Nguyen does not specifically teach initiating a timing period responsive to a target hardware access by the target processor.

12.6. Nguyen does not specifically teach detecting if the control signal is received from the physical hardware within a predetermined period after initiating the timing period.

12.7. Mano appears to teach monitoring a terminal on the target processor that is adapted to receive a control signal from the physical hardware by the target processor *(page 418 - 420, section labeled "Handshaking")*.

12.8. Mano appears to teach initiating a timing period responsive to a target hardware access by the target processor *(page 419 - 420, section labeled "Handshaking")*.

12.9. Mano appears to teach detecting if the control signal is received from the physical hardware within a predetermined period after initiating the timing period *(page 419 - 420, section labeled "Handshaking")*.

12.10.   Nguyen and Mano are analogous art because they both contain the

problem of sending data from a source device to a destination device.

12.11.   The motivation to combine the art of Mano with the art of Nguyen

would have been obvious given the statement in Mano that the

handshaking scheme of data transfer provides the benefits of a high

degree of reliability and flexibility *(page 419, text)*, and the recited

disadvantages of data transfer using the strobe method *(page 418,*

section labeled "Handshaking", first paragraph).

12.12.   Therefore, as discussed above, it would have been obvious to the

ordinary artisan at the time of invention to use the art of Mano with the

art of Nguyen to produce the invention of claim 26.

13.   Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Nguyen (U.S. Patent 5,790,881) in view of Mano (Mano, M. Morris;

"Computer System Architecture", 1982, Prentice-Hall).

13.1. Claim 27 is a dependent claim of claim 22, and thereby inherits all of

the rejected limitations of claim 22.

13.2. The art of Nguyen is directed toward a computer system including

coprocessor devices simulating memory interfaces *(Title)*.

13.3. The art of Mano is directed to computer system architecture *(Title)*.

13.4. Nguyen does not specifically teach detecting an interrupt signal

applied to the target processor during the time that the target processor

has suspended execution of the target program.

13.5. Nguyen does not specifically teach executing an interrupt routine

responsive to the interrupt signal.

13.6. Mano appears to teach detecting an interrupt signal applied to the

target processor during the time that the target processor has

suspended execution of the target program *(page 263, section labeled*

"Types of Interrupts", refer to the discussion of external

interrupts).

> **13.6.1.**   Regarding *(page 263, section labeled "Types of*
>
> *Interrupts", refer to the discussion of external interrupts)*; it is
>
> inherent that an external interrupt is allowed to occur during the
>
> time that the target processor has suspended execution of the target
>
> program.

13.7. Mano appears to teach executing an interrupt routine responsive to

the interrupt signal *(page 261, section labeled "Program Interrupt")*.

13.8. Nguyen and Mano are analogous art because they both contain the

problem of processing interrupts *(Nguyen, column 1, lines 35 – 37)*.

13.9. The motivation to combine the art of Mano with the art of Nguyen

would have been obvious given the statement in Mano that external

interrupts come from I/O devices, timing devices, or any other external

source *(page 263, section labeled "Types of Interrupts", refer to the*

discussion of external interrupts), which are common elements in a

computer system.

13.10.   Therefore, as discussed above, it would have been obvious to the

ordinary artisan at the time of invention to use the art of Mano with the

art of Nguyen to produce the invention of claim 27.

14.   Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Nguyen (U.S. Patent 5,790,881) in view of Mano (Mano, M. Morris;

"Computer System Architecture", 1982, Prentice-Hall), further in view of

Habinc (Habinc, Sandi; Sinander, Peter; "Using VHDL for Board Level

Simulation", 1996, Design and Test of Computers, IEEE, Volume 13, Issue

3).

14.1. Claim 28 is a dependent claim of claim 22, and thereby inherits all of

the rejected limitations of claim 22.

14.2. The art of Nguyen is directed toward a computer system including

coprocessor devices simulating memory interfaces *(Title)*.

14.3. The art of Mano is directed to computer system architecture *(Title)*.

14.4. The art of Habinc is directed to simulation of board level designs

(Title).

14.5. Nguyen does not specifically teach detecting data from the hardware

simulator corresponding to an interrupt signal.

14.6. Nguyen does not specifically teach in response to detecting data from

the hardware simulator corresponding to an interrupt signal, applying

an interrupt signal to the target processor.

14.7. Nguyen does not specifically teach in response to the interrupt signal,

allowing the target processor to execute an interrupt routine.

14.8. Habinc appears to teach detecting data from the hardware simulator

corresponding to an interrupt signal *(page 68, left-most column, the*

sentence that begins with "Figure 1 shows . . ." and the remainder

of the column, and page 68, figure 1, the box containing

interrupts).

14.9. Habinc appears to teach in response to detecting data from the

hardware simulator corresponding to an interrupt signal, applying an

interrupt signal to the target processor *(page 68, left-most column, the*

sentence that begins with "Figure 1 shows . . ." and the remainder

of the column, and page 68, figure 1, the box containing

interrupts).

14.10.   Mano appears to teach in response to the interrupt signal, allowing

the target processor to execute an interrupt routine **_(page 261, section_**

labeled "Program Interrupt").

14.11.   Nguyen and Mano are analogous art because they both contain the

problem of processing interrupts **_(Nguyen, column 1, lines 35 – 37)_**.

14.12.   Nguyen and Habinc are analogous art because they both contain

the problem of simulating computer components **_(Nguyen, Title)_**, and

(Habinc, Title).

14.13.   The motivation to combine the art of Mano with the art of Nguyen

would have been obvious given the statement in Mano that external

interrupts come from I/O devices, timing devices, or any other external

source **_(page 263, section labeled "Types of Interrupts", refer to the_**

discussion of external interrupts), which are common elements in a

computer system.

14.14.   The motivation to combine the art of Habinc with the art of Nguyen

would have been obvious given the statement in Habinc that board level

simulation allows designers to test a design early and verify interfaces

(page 66, right-most column, third paragraph), and further, that

prototyping is necessary for successful development of printed circuit

boards with complex components **_(page 66, center box)_**.

14.15. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano and Habinc with the art of Nguyen to produce the invention of claim 28.
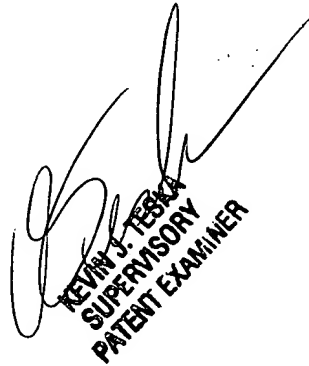
Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM – 5:30 PM.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

17.   Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status

information for published applications may be obtained from either Private

PAIR or Public PAIR. Status information for unpublished applications is

available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center

(EBC) at 866-217-9197 (toll-free).

RG